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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,541	07/30/2003	Shinichi Abe	KY-190	6516

7590 11/30/2005

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EXAMINER	
KOVALICK, VINCENT E	

ART UNIT	PAPER NUMBER
2677	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,541	ABE ET AL.	
	Examiner	Art Unit	
	Vincent E. Kovalick	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2 and 11* is/are rejected.

7)☒ Claim(s) *3-10 and 12-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Patent Application, Serial No. 10/629,541, with a File date of July 30, 2003 and Applicant's Preliminary Amendment dated April 20, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al. (Pub. No US 2001/0026251); taken with Yamada et al. (USP 5,990,629); in view of Kaneko et al. (USP 6,323,847) taken with Traa (USP 4,991,119).

Relative to claims 1 and 11, Hunter et al. **teaches** a display device having current-addressed pixels (pg. 1, paras. 0001-0016); Hunter further **teaches** a drive circuit of an active matrix type organic EL display panel, for current-driving an active matrix type organic EL display panel having a plurality of pixel circuits arranged in matrix, each said pixel circuit including an organic EL element (pg. 2, para 0032); Hunter further **teaches** a plurality of current drive circuits each provided for a data line or a column pin of said organic EL display panel, each said current drive circuit having an output pin connected to said data line or said column pin and

generating a current for charging said capacitor of each said pixel circuit through said data line or said column pin and a current for initially charging said organic EL element (pg. 2, para 0032).

Hunter et al. **does not teach** a capacitor for storing a voltage value corresponding to a value of a drive current of said organic EL element and a plurality of transistors for supplying the drive current to said organic EL element correspondingly to the voltage value.

Yamada et al. **teaches** an electroluminescent display device and driving method thereof (col. 2, lines 10-67 and col. 3, lines 1-67); Yamada et al. further **teaches** a capacitor for storing a voltage value corresponding to a value of a drive current of said organic EL element and a plurality of transistors for supplying the drive current to said organic EL element correspondingly to the voltage value (col. 33, lines 10-26).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Hunter et al. the feature as taught by Yamada et al. in order to put in place the means to store and supply the current to drive the EL device when the system addresses the particular EL device.

Hunter et al. taken with Yamada et al. **does not teach** a write control circuit for controlling a write for storing the voltage value in said capacitor and for controlling and resetting the written voltage value of said capacitor.

Kaneko et al. **teaches** a liquid crystal display which can provide a high-quality image by using a simple circuit structure (col. 2, lines 1-67; col. 3, lines 1-67 and col. 4, lines 1-43); Kaneko et al. further teaches a write control circuit for controlling a write for storing the voltage value in said capacitor (col. 2, lines 40-47).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Hunter et al. taken with Yamada et al. the feature as taught by Kaneko et al. in order to put in place the means for storing voltage values in the pixel circuit capacitor.

Hunter et al. taken with Yamada et al. in view of Kaneko et al. **does not teach** a control circuit for controlling and resetting the written voltage value of said capacitor.

Traa **teaches** a picture display device (col. 1, lines 63-68 and col. 2, lines 1-50); Traa further **teaches** a control circuit for controlling and resetting the written voltage value of said capacitor (col. 3, lines 61-62).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Hunter et al. taken with Yamada et al. in view of Kaneko et al. the feature as taught by Traa in order to put in place the means for resetting the voltage values of the

pixel circuit capacitor.

Regading claim 2, Hunter et al further teaches a said drive circuit of an active matrix type organic EL display panel wherein, in order to charge said capacitor of said pixel circuit connected to each said current drive circuit to the voltage value through said output pin within a short time, each said current drive ciucuit comprises a charging circuit for generating a current or a voltage for initially charging said capacitor (pg. 5, para 0070).

Allowable Subject Matter

4. Claims 3-10 and 12-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 3, the major difference between the teachings of the prior art of record (Pub. No. US 2001/0026251, Hunter et al.; USP 5,990,629 Yamada et al. and USP 6,323,847 Kaneko et al.) and that of the instant invention is that said prior art of record **does not teach** a drive circuit of an active matrix type organic EL display panel wherein the current for charging said capacitor to the voltage value is generated correspondingly to one of a current pulled out from said output pin to said pixel circuit and a current pulled in from said pixel circuit to said output pin and the current for initially charging said organic EL element is generated correspondingly to one of another current pulled out from said output pin to said pixel circuit and another current pulled in form said pixel circuit to said output pin.

Relative to claim 15, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** an organic EL display device wherein the pixel circuit includes a first, second, third and fourth P channel MOS transistor, a gate and drain of said first transistor are connected to a selection line and said data line, respectively, at a cross pint of said selection line and said data line, a source of said first transistor is connected to a gate of said third transistor through a drain-source of said second transistor, said capacitor is connected between a source and gate of said third transistor, said source of said third transistor is connected to a power source line, a drain of said third transistor

is connected to a source of said fourth transistor and a drain of said fourth transistor is connected to an anode of said organic EL element.

Relative to claim 18, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** an organic EL display device wherein said pixel circuit includes a series circuit composed of a first and second MOS transistors for driving said organic EL element and a third and fourth MOS transistors for writing the voltage value in said capacitor, said capacitor is connected between a gate of said first MOS transistor and one of a source and a drain of said first MOS transistor, one of a source and a drain of said second MOS transistor is connected to an anode of said organic EL element, said third MOS transistor in connected between a gate of said first MOS transistor and the other of said source and drain of said first MOS transistor, said fourth MOS transistor is connected between the other of said source and drain of said first MOS transistor and said output pin of said current drive circuit, one of said gates of said second and third MOS transistors is connected to the other gate through an inverter, and said write control circuit performs the write control by supplying control signals to said gate of said fourth MOS transistor and said gate connected to an input side of said inverter to NO/OFF control said second, third and fourth MOS transistors.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,246,384	Sano
U. S. Patent No.	5,078,236	Miyake
U. S. Patent No.	5,812,104	Kapoor et al.
Pub. No. US	2002/0063672	Stevens
Pub. No. US	2001/0055008	Young et al.

To Respond

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent E. Kovalick
November 18, 2005

AMR A. AWAD
PRIMARY EXAMINER